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Attorney's Docket No.: Intel 10559-108001 / P7643

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Keith Dow
Serial No.: 09/461,643
Filed : December 14, 1999

Art Unit: 2112
Examiner: Christopher E. Lee
Assignee: Intel Corporation

Title : IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Total Claims	19	-	22	=	0	$0
Independent	4	-	4	=	0	$0
Appeal Brief Fee						$330
TOTAL FEE DUE						$330

Respectfully submitted,

Date: March 12, 2004

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Carroll Allman
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BRIEF ON APPEAL

Applicant herewith files this brief on appeal thus perfecting the Notice of Appeal originally filed on March 10, 2004. The headings and content required by 37 C.F.R. § 192 follow.

(1) Real Party in Interest

The application is assigned to Intel Corporation.

(2) Related Appeals and Interferences

There are no known appeals or interferences related to the above-identified patent application.

(3) Status of Claims

This is an appeal from the Office action dated January 7, 2004, finally rejecting claims 1, 3-8, 10-14, 16-20, 23 and 24, all the pending claims of the above application. Claims 1, 4-8,

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11-14, 16-20, 23 and 24 stand rejected under 35 U.S.C. §103(a) as obvious over the prior art admitted by the appellant (hereinafter "AAPA") and U.S. Patent 6,160,716 to Perino et al. (hereinafter "Perino"). Claims 3 and 10 stand rejected under 35 U.S.C. §103(a) as obvious over the AAPA, Perino, and U.S. Patent No. 4,904,968 to Theus (hereinafter "Theus").

(4) Status of Amendments

No response to the final Office action dated January 7, 2004 was filed. All amendments have been entered.

(5) Summary of Invention

BACKGROUND

The speed at which a computer operates depends in large part on the speed at which data is transferred amongst the computer's constituent components. Two such components are the computer processor and the computer memory, which communicate over a memory control unit that controls the flow of data into and out of the memory. See, e.g., FIG. 1 and page 1, line 9-22 of the specification.

Often, a single terminal of a memory unit must exchange data with multiple elements in order for such data communication to occur. This generally requires the routing of a pair of signal lines to an individual data terminal. The prior art shows a circuit board where a pair of signal lines obliquely approach an individual terminal at an acute angle. The signal lines "neck down" (i.e., reduce in width) as they approach the terminal and are separated by a ground trace. See, e.g., *id.* FIG. 2 and page 2, line 4-16.

The necking down of the signal lines and the intervening ground trace (as well as other geometric and material properties) define the electrical characteristics in the vicinity of the data terminal. These electrical characteristics include the electrical impedance in the vicinity of the data terminal as well the capacitance between the signal lines. When designed properly, these electrical characteristics can allow the memory control unit to exchange data at the high frequencies required in modern computer systems.

THE PRESENT INVENTION

The inventor has recognized that, although the electrical characteristics of the prior art allows such data transfer to occur, the prior art has certain deficiencies. For example, due to the congestion of lines (including the ground trace) in the vicinity of such data terminals, the signal lines must often be formed on different layers of the circuit board. Routing the signal lines in this manner increases both the number of required layers and the cost of the circuit board.

The inventor has described a routing configuration for a circuit board in a computer system where the electrical characteristics in the vicinity of a data terminal allow high frequency data transfer to occur but yet the congestion of lines in the vicinity is reduced. Such a circuit board can include at least two layers. With reference to FIG. 3, on the same first layer, a pair of signal lines (namely, a first signal line 200 and a second signal line 210) can be formed. See *id.*, page 4, line 16-18. A first portion of the second signal line (the top of 215) is routed at an acute angle relative to a first portion of the first signal line (the top of 205). See *id.*, page 4, line 5-8. A second portion of the second signal line (the

bottom of 215) is routed substantially parallel to a second portion of the first signal line (the bottom of 205). See *id.*, page 4, line 5-8. A non-grounded gap 220 is defined between said first and second portions of the first and second lines. See *id.*, page 4, line 8-16.

With such a routing configuration, the congestion in the vicinity of the terminal may be reduced. The signal lines can be routed on a single layer of the circuit board, reducing the number of layers and the cost of the circuit board.

(6) Issues

The issues to be decided on appeal are:

Are the claims properly rejected under 35 U.S.C. §103(a) as obvious over the AAPA in view of Perino?

(7) Grouping of Claims

Claims 1, 3-7, 20 and 23-24 stand or fall with independent claim 20.

Claims 8 and 10-13 stand or fall with independent claim 8.

Claims 14 and 16-19 stand or fall with independent claim 14.

(8) Argument

It is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. §103(a) of claims 1, 8, 14, and 20 has not been established.

CLAIM 20

The Examiner and the appellant agree that both the AAPA and Perino individually fail to describe or suggest signal lines as recited in claim 20. Both claims recite first and second signal lines that have the following characteristics:

Char. 1) each is "connected to the first pin on the memory unit;"

Char. 2) each is "formed on the first layer of the circuit board;"

Char. 3) each includes a "first portion of the second signal line at an acute angle relative to a first portion of the first signal line;"

Char. 4) each includes a "second portion" that is "substantially parallel" to a "second portion" of the other signal line; and

Char. 5) a "first layer defines a non-grounded gap between the first and second portions of the first and second lines."

The Examiner and the appellant agree that neither the AAPA nor Perino individually describe or suggest such signal lines.

The issue at hand is whether or not particular characteristics of signal lines described in the AAPA and particular characteristics of signal lines described in Perino would be selected by one of ordinary skill for combination to arrive at the claimed signal lines. The rejection contends that one of ordinary skill would find a suggestion to combine characteristics 1) and 3), drawn from the AAPA, with characteristics 2), 4), and 5), drawn from Perino. Appellant respectfully submits that the proposed combination represents improper hindsight-based reconstruction of the claimed signal lines is improper for at least the following reasons:

1) Perino expressly teaches signal lines are not to be connected;

2) Perino expressly teaches away from a non-grounded gap between signal lines; and

3) there is no suggestion to combine and/or a reasonable expectation of success founded in the prior art.

Appellant therefore respectfully submits that the proposed combination ignores the teachings of Perino as a whole and amounts to hindsight-based reconstruction of the claims.

1) Perino expressly teaches away from the claimed connection of signal lines

Perino expressly teaches away from connecting signal lines to the same pin. Every signal line in Perino is routed around pins that are connected to another single signal line. See, e.g., FIGS. 4, 7, 11, and 16 of Perino. Indeed, according to Perino, each signal line should not come close to, much less connect with, another signal line. "Closely spaced traces 130 may cause interference in some instances, or actual contact between the traces 130 if the traces are imperfectly fabricated." Perino, col. 2, lines 15-22. Indeed, the connection of Perino's parallel signal lines to a single pin will destroy the efficacy of Perino's device. One of ordinary skill who reads Perino would obtain the teaching that lines connected to a single pin are a manufacturing defect rather than a desirable result.

"A reference may be said to teach away when a person of ordinary skill, upon reading the reference, … would be led in a

direction divergent from the path that was taken by the appellant." In re Gurley, 27 F.3d 551 (Fed. Cir. 1994).

Moreover, the rejection contends that one of ordinary skill would be motivated, not only to ignore the express teachings of Perino away from characteristics of the claimed invention, but also to pick and choose some particular characteristics of Perino's signal lines while discarding others to arrive at the claimed invention. The Examiner contends that one of ordinary skill would do so "for the advantage of … eliminating reflected signals and signal deterioration caused by a mismatched impedance." See page 4, line 6-8 of the action mailed January 7, 2004 (stated twice) (citing col. 5, line 29-32 of Perino).

However, Perino achieves the cited elimination of reflected signals and mismatched impedance by maximizing the width of traces to reduce the impedance of those traces. See, e.g., col. 5, line 21-22 ("Maximizing the width of the traces … decreases the impedance of the traces."); col. 5, line 29-30 ("Reducing impedance of the traces … to match low impedance lines/signals is advantageous because a matched impedance eliminates reflected signals, and signal deterioration."). The motivation relied on in the rejection thus provides a rationale for maximizing the width of signal lines rather than achieving the proposed combination.

Therefore, the purported motivation relied on in the rejection is irrelevant to the suggested combination. To achieve Perino's asserted advantages of eliminating reflected signals and signal deterioration caused by a mismatched impedance, one of ordinary skill would follow Perino's teachings and maximize the width of traces. One would not, as contended, connect Perino's signal lines to the same first pin and discard

Perino's express teachings regarding the undesirability of such a connection.

Since, when considered in its entirety, Perino expressly teaches away from connecting signal lines to a single pin and provides no suggestion to combine relevant to the proposed combination with the AAPA, it is respectfully submitted that a *prima facie* case of obviousness has not been established.

2) Perino teaches away from a non-grounded gap between signal lines

Perino further teaches away from signal lines being separated by a non-grounded gap. Attention is respectfully directed to FIG. 11 and the written description thereof, where Perino teaches away from signal lines separated by a non-grounded gap and instead describes the advantages of ground traces 1160 intervening between signal lines 1170. "[G]round traces 1160 prevent interference." "[G]round traces 1160 reduce mutual capacitance and mutual inductance." "[B]y placing ground traces 1160 … between the signal traces 1170, noise is reduced." Perino, col. 6, line 14-21. These provide clear teachings that the gap between the traces should be grounded. These teachings are ignored by the rejection.

In addition to ignoring these teachings, the rejection also contends that one of ordinary skill would be motivated to pick and choose some particular characteristics of Perino's signal lines while discarding others to arrive at the claimed invention. In particular, the Examiner once again contends that one of ordinary skill would do so for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance. As discussed above, a close reading of

Perino reveals that the motivation relied on in the rejection only provides a rationale for maximizing the width of signal lines and not, as contended, for separating signal lines by a non-grounded gap or discarding Perino's express teachings regarding the undesirability of a non-grounded gap.

The Examiner also contends that, since the rejection does not rely upon FIG. 11 in rejecting the claims (and instead relies upon FIGS. 8 and 16), that Perino's teaching regarding FIG. 11 are irrelevant to any proposed combination involving Perino. Contrary to this assertion, applicant respectfully submits that Perino's teachings regarding the undesirability of a non-grounded gap are relevant to the present patentability determination. To begin with, in discussing FIG. 11, Perino is contrasting Perino's invention of FIG. 11 with the prior art illustrated in FIG. 8, where there are no ground traces intervening between traces 830, 840 and 870, 880. Perino's statements are thus express commentary on the embodiment shown in FIG. 8, which is the <u>exact portion</u> of Perino relied on in rejecting the claims.

In addition to this mistaken premise, the law requires that the totality of a reference's teachings must be considered when determining if a reference teaches away. Simply put, a reference's teaching cannot be picked out of context and combined with another reference using the appellant's claims as a guide. Rather, the references taken as a whole must suggest the combination to one of ordinary skill in the art. See, e.g., <u>In re Gorman</u>, 933 F.2d 982, 986 (Fed. Cir. 1991) ("[T]he test [for obviousness] is whether the combined teachings of the prior art, taken as a whole, would have rendered the claimed invention obvious to one of ordinary skill in the art.").

Since, when considered in its entirety, Perino expressly teaches away from separating signal lines using a non-grounded gap and provides no suggestion to combine relevant to the proposed combination with the AAPA, it is respectfully submitted that a *prima facie* case of obviousness has not been established.

3) There is no suggestion to combine and/or a reasonable expectation of success founded in the prior art

There is no suggestion to combine and reasonable expectation of success founded in the prior art. The suggested combination requires one of ordinary skill to select particular characteristics of the signal lines of Perino, discard other characteristics of Perino's signal lines, discard certain characteristics of the AAPA, and incorporate the characteristics selected from Perino into the AAPA in a specific manner. It is respectfully submitted that there is no suggestion to combine or reasonable expectation of success founded in the prior are that would lead one of ordinary skill to perform the proposed combination.

The proposed inclusion of substantially parallel portions in the signal lines of the AAPA is illustrative of how the proposed combination would have to proceed. The rejection contends that one of ordinary skill would specifically select the particular characteristic of signal lines having parallel portions from Perino, discard other characteristics of Perino's signal lines (including the characteristic of the parallel portions not contacting), discard characteristics of the signal lines in the AAPA, and then incorporate the characteristic of having a substantially parallel portion into the remainder of the signal lines of the AAPA to yield the claimed invention.

This incorporation would perforce have to include decisions as to how to incorporate the particular characteristic, such as a decision not to eliminate the first portions from the AAPA that are at an acute angle relative to each other.

The rejection contends that this combination is obvious to one of ordinary skill who would be motivated to eliminate reflected signals and signal deterioration caused by a mismatched impedance. As discussed above, a close reading of Perino reveals that the motivation relied on in the rejection only provides a rationale for maximizing the width of signal lines. Perino simply provides a rationale for maximizing the width of signal lines, which itself is not recommended given the problem of congestion in the vicinity of a single pin.

In the absence of a suggestion to combine, there is no indication in Perino that reflected signals and signal deterioration can be eliminated by selecting the characteristic of having a substantially parallel portion, ignoring express teachings in Perino in deciding to discard other characteristics of Perino's signal lines, and incorporating the substantially parallel portions into the signal lines in the manner claimed. Similarly, there is no indication in Perino that reflected signals and signal deterioration can be eliminated by the same process for combining the characteristics of being formed on the first layer of the circuit board and having a first layer defines a non-grounded gap between the first and second portions of the first and second lines into the AAPA. Rather, this is simply hindsight-based reconstruction of appellant's claims.

Moreover, Perino himself explicitly teaches that reflected signals and signal deterioration are <u>caused</u> by the structures in Perino relied on in rejecting the claims. "'[T]wo-between

routing' may cause interference between the signals carried by either of the traces." "[T]hin traces have an increased impedance, that does not match the impedance of the signals." Perino, col. 2, lines 15-33. FIG. 8, relied on in rejecting the claims, explicitly illustrates the prior art two-between routing disparaged by Perino. Two traces 830, 840 are routed between two contact areas 810, 820. Thus, according to Perino, the embodiment of FIG. 8 relied upon in rejecting claims 1 and 20 is <u>disadvantageous</u>.

The rejection contends that because the embodiment of FIG. 8 is engineered to minimize the impact of the impedance mismatch caused by two-between routing (i.e., the distances between traces 830, 840 and contact areas 810, 820 are minimized while the width of traces 830, 840 is maximized to decrease the impedance of traces 830, 840, as described in col. 5, line 19-21 of Perino), that one of ordinary skill would suddenly find this advantageous in contexts outside of two-between routing. By this logic, an approach to making the best of a bad situation would motivate one of ordinary skill even outside the context of the bad situation. In short, the rejection would have one of ordinary skill make lemonade even when life did not give one lemons.

It is therefore respectfully submitted that one of ordinary skill in the art would find no suggestion to combine Perino with the AAPA in the manner suggested and a *prima facie* case of obviousness has not been established.

Accordingly, Appellant submits that claim 20 and the claims standing or falling therewith are allowable.

CLAIM 8

Independent claim 8 was also rejected under 35 U.S.C. §103(a) as obvious over the AAPA and Perino. This rejection is respectfully traversed.

Claim 8 relates to a method for use in routing signals between a memory unit and a memory control unit. The method includes delivering a first signal over a first signal line on a first layer of a multi-layer circuit board and delivering a second signal over a second signal line formed on the same first layer. The first signal line is connected between a memory control unit and a first pin on the memory unit. The second signal line is connected to the first pin of the memory unit. The first and second signal lines include first and second portions similar to the portions of the signal lines in claim 20.

Even if one were to ignore the above-noted deficiencies of the combination of the AAPA and Perino to arrive at the signal lines in claim 20, claim 8 would still be patentable. Claim 8 is a method claim, and nothing in either the AAPA and Perino describes or suggests the method steps of delivering signals over two signal lines that are both on a first layer of a circuit board and connected to a pin of a memory unit. In the AAPA, signals are to be delivered over signal lines on different layers to accommodate congestion in the vicinity of a pin. In Perino, signals are to be delivered over signal lines that do not contact the same pin.

Therefore, neither the AAPA nor Perino describes or suggests delivering signals as claimed. Accordingly, Appellant submits that claim 8 and the claims standing or falling therewith are allowable.

CLAIM 14

Independent claim 14 was rejected under 35 U.S.C. §103(a) as obvious over AAPA and Perino. This rejection is respectfully traversed.

Claim 14 relates to a method for use in manufacturing a computer system. The method includes forming a first layer of a circuit board with first and second signal lines thereon and connecting a memory unit to the board such that a first pin on the memory unit connects to the first and second signal lines. The method also includes forming signal lines similar to the signal lines of claim 20.

Even if one were to ignore the above-noted deficiencies of the combination of AAPA and Perino to arrive at the signal lines in claim 20, claim 14 would still be patentable. Claim 14 is a method claim, and nothing in either the AAPA and Perino describes or suggests the method steps of forming a first layer with first and second signal lines thereon and connecting a memory unit such that a first pin connects to the first and second signal lines.

In the AAPA, two different layers are to be formed with signal lines to accommodate congestion in the vicinity of a pin. In Perino, signal lines that are to be formed so that they do not contact the same pin. Therefore, neither AAPA nor Perino describes or suggests forming the first layer or connecting a memory unit as claimed. Accordingly, Appellant submits that claim 14 and the claims standing or falling therewith are allowable.

The brief fee of $330 is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: March 12, 2004

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Appendix of Claims

Claim 1. (Previously Presented) A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit; and

a circuit board comprising:

at least two layers formed in parallel to a surface of said circuit board,

a first signal line, formed on a first layer of the circuit board and connected between a first pin on the memory unit and the memory control unit, and

a second signal line also formed on the first layer of the circuit board and connected to the first pin on the memory unit, a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line,

wherein said first layer defines a non-grounded gap between said first and second portions of the first and second lines.

Claim 2. (Canceled)

Claim 3. (Original) The system of claim 1, further comprising third and fourth signal lines, on a second layer of the circuit board, different than the first layer.

Claim 4. (Previously Presented) The system of claim 1, wherein the second portion of the first signal line and the second portion of the second signal line have substantially equal widths.

Claim 5. (Previously Presented) The system of claim 4, wherein the second portion of the first signal line and the second portion of the second signal line are separated by a perpendicular distance substantially equal to said widths.

Claim 6. (Currently Amended) The system of claim 5, wherein the widths of the lines and the perpendicular distance separating the second portions of the lines are each substantially equal to 5 mils.

Claim 7. (Previously Presented) The system of claim 1, wherein the memory unit comprises a RAMBUS™ device.

Claim 8. (Previously Presented) A method for use in routing signals between a memory unit and a memory control unit,

the method comprising:

delivering a first signal over a first signal line on a first layer formed in parallel to a second layer on a surface of a multi-layer circuit board and connected between the memory control unit and a first pin on the memory unit;

delivering a second signal over a second signal line formed on the first layer of the circuit board and connected to the first pin of the memory unit, a first portion of the second signal line formed at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line formed substantially parallel to a second portion of the first signal line,

said first and second portions of the first and second signal lines separated without a ground connection therebetween.

Claim 9. (Canceled)

Claim 10. (Previously Presented) The method of claim 8, further comprising delivering another signal to said memory control unit on another parallel layer of the circuit board over portions of the first and second signal lines that are not separated by any conductive traces.

Claim 11. (Previously Presented) The method of claim 8, wherein delivering the first signal and the second signal includes delivering the signals over second portions of the first and second signal lines that have substantially equal widths.

Claim 12. (Previously Presented) The method of claim 11, wherein delivering the first signal and the second signal includes delivering the signals over second portions of the first and second signal lines that are separated by a perpendicular distance substantially equal to their widths.

Claim 13. (Previously Presented) The method of claim 12, wherein delivering the first signal and the second signal includes delivering the signals over second portions of the first and second signal lines that are substantially equal to 5 mils wide and that are separated by a perpendicular distance substantially equal to 5 mils.

Claim 14. (Previously Presented) A method for use in manufacturing a computer system, the method comprising:

forming at least two layers parallel to a surface of a circuit board, with first and second signal lines on a first layer of the board;

connecting a memory unit to the board such that a first pin on the memory unit connects to the first and second signal lines;

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line;

forming a first portion of the second signal line to be at an acute angle relative to a first portion of the first signal line; and

forming a second portion of the second signal line to be substantially parallel to a second portion of the first signal line.

Claim 15. (Canceled)

Claim 16. (Previously Presented) The method of claim 14, further comprising forming the first and second signal lines such that no conductive trace lies between the second portion of the first signal line and the second portion of the second signal line.

Claim 17. (Previously Presented) The method of claim 16, further comprising forming the second portion of the first signal line and the second portion of the second signal line to have substantially equal widths.

Claim 18. (Previously Presented) The method of claim 17, further comprising forming the second portion of the first signal line and the second portion of the second signal line to be separated by a perpendicular distance approximately equal to their widths.

Claim 19. (Previously Presented) The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the perpendicular distance separating the second portions of the lines are all substantially equal to 5 mils.

Claim 20. (Previously Presented) A circuit board comprising at least two layers formed in parallel to a surface of said circuit board for use in a computer system comprising:

a memory unit;

a memory control unit; and

a data bus connecting the memory control unit to the memory unit and comprising:

a first signal line formed on a first layer of the circuit board and connected to the memory control unit and to a first pin on the memory unit, and

a second signal line formed on the first layer of the circuit board and also connected to the first pin connection on

the memory unit, a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line,

wherein the widths of the lines and a perpendicular distance separating the second portions of the lines are each substantially equal, and

wherein said first layer defines a non-grounded gap between said first and second portions of the first and second lines.

Claims 21-22. (Canceled)

Claim 23. (Previously Presented) The computer system of claim 1, wherein the memory unit comprises a memory repeater hub.

Claim 24. (Previously Presented) The circuit board of claim 20, wherein the memory unit comprises a memory repeater hub.